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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,413	11/10/2003	Hiroyuki Morishita	82478-1800	5180

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/705,413	MORISHITA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on December 06, 2006. This amendment has been entered and carefully considered. Claims 8-9 and 11 are cancelled. Therefore, claims 1-7, 10 and 12-17 are currently pending in this application.

2. Applicant's arguments filed on December 06, 2006 have been fully considered but they are not deemed to be persuasive in view of new grounds of rejection.

Claim Rejections - 35 USC § 103

3. Claims 1-3, 10 and 12-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy ("The Cache Memory book") in view of Suh et al. ("Dynamic Cache Partitioning for Simultaneous Multithreading Systems") further in view of Stevens (USPN: 6,745,292).

Regarding claims 1, and 14-17, Handy shows that a computer with a cache, main memory, a microprocessor, an address receiving unit, a caching unit to acquire the data block from main memory (pg 12, 51, and 52), having the address converting unit convert the logical address to the physical address, sending the address to the receiving unit, and storing the physical address in the cache were well known in the art (pg 12 and 52). Furthermore, Handy further shows an address receiving unit to receive a logical address, a data block managing unit to manage data stored in the cache using the logical addresses, and an address converting unit to convert the address to the physical address and sent it to main memory (pg 12 and 52). However, Handy does not

expressly show a region-managing unit to manage regions in the cache. Suh et al. does teach the use of a region-managing unit that manages regions in cache. Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-17.

However, none of them are teaching the further limitation of having a judging unit as claimed. Stevens, on the other hand, teaches about judging whether the requested data is stored in the cache memory by searching all of the plurality of regions in the cache memory (i.e. by searching all regions (Reg. 0 – Reg. 3 shown in Figs. 2 and 3b) when the cache miss occurs). Stevens clearly discloses in abstract that "All the processors have access to all regions on hits" (e.g. see the Abstract and Col. 1, lines 36-40). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the judging function taught by Stevens in the cache controller taught by the combination of Handy and Suh. In doing so, the number of cache miss is reduced by getting the cache hit for the requested data not present in the requesting cache region but present in any other cache region(s) within the entire cache. Therefore, the performance of the computer system increases.

Regarding claims 2 and 3, Suh et al. goes on to further describe that the region managing unit divides the cache into a plurality of regions equal to the number of tasks

and finds out how many tasks are running and divides the cache based on the information. Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for these features of dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-16.

Regarding claim 10, the combination of Handy and Suh teaches the claimed invention as described above and furthermore, Handy discloses that the cache memory is made of a plurality of ways, and the plurality of regions each contain at least one way. Handy also teaches about using set associative mapping for each region containing more than one way (e.g. see pgs 53-55).

Regarding claim 12, Handy, Stevens and Suh et al. describe all the limitations of claim 1 and furthermore, Stevens discloses about dividing the cache memory into a specific region (i.e. the cache memory region 0 associated with the processor 0) and a nonspecific region (i.e. the the combination of cache memory regions 1-3 associated with the processors 1-3), and manages the specific region in correspondence with a specific task out of the plurality of tasks (i.e. a task executed by the processor 0), and the caching unit stores the acquired data block into the specific region if the task is the specific task (i.e. the acquired data of processor 0 is stored in the cache memory region 0), and into the nonspecific region if the task is other than the specific task (i.e. the

acquired data of other than processor 0 is not stored in the cache memory region 0 but stored in the combination of cache memory regions 1-3 associated with the processors 1-3) (e.g. see the Abstract and Col. 1, lines 36-40 and Figs. 2-3).

Regarding claim 13, Handy, Stevens and Suh et al. describe all the limitations of claim 1 and furthermore, Stevens discloses the microprocessor concurrently executes a first task (i.e. the task executed by the processor 0), a second task (i.e. the task executed by the processor 1), and a third task (i.e. the task executed by the processor 2), the region managing unit divides the cache memory into a first region (i.e. the combination of cache memory regions 0, 1 and 3 associated with the processors 0, 1 and 3) and a second region (i.e. the cache memory region 2 associated with the processor 2), and manages the first region in correspondence with the first task and the second task, and the second region in correspondence with the third task, and the caching unit stores the acquired data block into the first region if the task is the first task or the second task, and into the second region if the task is the third task (e.g. see the Abstract and Col. 1, lines 36-40 and Figs. 2-3).

4. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al. and Stevens as applied to claims 1-3 above, and further in view of Patterson et al.

Regarding claim 4, Handy, Suh et al. and Stevens described all of the limitations of claims 1-3 and Suh et al. further describes having the region management unit managing a plurality of regions in a one-to-one correspondence with task (process)

identifiers. Neither of Handy, Suh et al. and Stevens expressly describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier. Patterson et al. does describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier. Handy, Suh et al., Stevens and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al. and Handy for the benefit of classification to obtain the invention as specified in claim 4.

Regarding claim 7, Patterson et al. shows that the task identifier could be a process identifier assigned and ran by the operating system (pg 598) and evidentiary support shows that a microprocessor that could perform multitasking under the control of an operating system for a while (Review of operating systems). Handy, Suh et al., Stevens and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al., Stevens and Handy for the benefit of classification to obtain the invention as specified in claim 7.

5. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al., Stevens and Patterson et al. as applied to claims 1-4 above, and further in view of Thaler et al. (Pat No 5983329).

Handy, Suh et al., Stevens and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose the task identifier being an address of the data location in main memory. Thaler et al. does describe the task identifier being the address of the data location in main memory (column 4, lines 38-46). Handy, Suh et al., Stevens, Patterson et al. and Thaler et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the task identifier be the address of the data in main memory. The suggestion for doing so would have been to save cache space while still uniquely identifying all data in the cache. Therefore, it would have been obvious to combine Handy, Suh et al., Stevens, Patterson et al. and Thaler et al. for the benefit of saved space to obtain the invention as specified in claim 5.

6. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al., Stevens and Patterson et al. as applied to claims 1-4 above, and further in view of Hum et al. (Pub No 20020087824).

Handy, Suh et al., Stevens and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose that the task identifier is generated by

converting an address of a location in the main memory at which the task is stored as a program. Hum et al. does disclose the task identifier is generated by converting an address of a location in the main memory at which the task is stored as a program (paragraph 16). Handy, Suh et al., Stevens, Patterson et al. and Hum et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the task identifier be a derivation of the address of the data in main memory. The suggestion for doing so would have been to have a unique identifier for each set of data in the cache while still being able to extract the address of the data in main memory and thus saving space. Therefore, it would have been obvious to combine Handy, Suh et al., Stevens, Patterson et al. and Hum et al. for the benefit of space saving to obtain the invention as specified in claim 6.

Response to Arguments

7. As to the remark, Applicant asserted:

(a) Applicant's cache controller features a judgment unit that searches all of the cache memory regions to determine if the cache memory has a data block needed by the microprocessor. The judgment unit has a cache "hit" when the needed data block is in any of the cache regions and the judgment unit has a cache "miss" when the needed data block is not in any of the cache regions. The Office Action asserts that Chiou teaches "searching all the column caches when the miss occurs," (Office Action, Page 3, Lines 14-15). Applicant submits this is a

misstatement of Chiou's teaching. Chiou does not teach "searching all column caches when the miss occurs".

(b) The Office Action relies on Chiou as the linchpin for the obviousness rejection. Yet the Office Action fails to show the motivation to combine the prior art teachings in the manner claimed. The Office Action merely extols one of the virtues of Applicant's combination (i.e. increased performance) (Office Action, Page 3, Lines 19-20).

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Examiner agreed with Applicant about the Chiou prior art not teaching the claimed limitation. However, Stevens teaches about judging whether the requested data is stored in the cache memory by searching all of the plurality of regions in the cache memory (i.e. by searching all regions (Reg. 0 – Reg. 3 shown in Figs. 2 and 3b) when the cache miss occurs). Stevens clearly discloses in abstract that "All the processors have access to all regions on hits" (e.g. see the Abstract and Col. 1, lines 36-40).

With respect to (b), in response to applicant's argument that the office action simply extols one of the virtues of Applicant's combinations, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed.

Cir. 1992). In this case, the motivation to combine the Chiou prior art with other prior art(s) comes from the knowledge generally available to one of ordinary skill in the art at the time of the current invention was made. In other words, it would be in the knowledge generally available to one of ordinary skill in the art that the performance of the computer system would increase if the number of cache miss is lowered by getting the cache hit for the requested data not present in the requesting column cache (i.e. the cache region) but present in any other column cache within the entire cache.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H.B.Patel 01/08/2007
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Art Unit 2186